Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-46. (Canceled).

47. (Currently Amended) An optical logic circuit performing an inversion function, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate the optical layer comprising a second material, the optical layer configured to provide a plurality of optical pathways, the optical pathways forming an ~~a plurality of~~ optical logic gate ~~gates~~, ~~at least some of~~ the optical logic gate ~~gates~~ having a first input that receives a constant coherent light input from a light source, a second input that receives a coherent light input which can be selectively turned on and off, an interference region coupled to the first and second light inputs, and an output coupled to the interference region opposite the first and second light inputs;

the interference region comprises the second material and is bounded on ~~its periphery~~ all sides by material other than the second material except where the first and second optical inputs and optical output are located, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the optical inputs and the optical output ~~the periphery being a single, outer periphery such that only the interference region is within the periphery~~, the first and second optical inputs are spaced apart and the output is positioned along a chosen line, ~~of many lines,~~ along which maximum destructive interference occurs when the light input at the second input is on, the maximum destructive interference being caused exclusively by the interaction between first and second light inputs,

wherein the optical output signal is a Boolean logic output signal based on the second optical input signal, the optical output signal exits the interference region output, and the

output signal having one of two intensities, either a substantially on or a substantially off intensity.

48. (Previously Presented) The optical logic circuit of claim 47, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region through the output when the coherent light input to the second input is turned on.

49. (Previously Presented) The optical logic circuit of claim 47, wherein the interference region includes a third optical input receiving a coherent light input signal which can be selectively turned on and off.

50. (Previously Presented) The optical logic circuit of claim 49, wherein the interference region is configured to cause substantial cancellation of light exiting the output when coherent light is provided to the interference region through both the second optical input and the third optical input.

51. (Previously Presented) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT (inverter) function.

52. (Currently Amended) The optical logic circuit of claim ~~47~~ 49, wherein the Boolean logic output is a NOT AND (NAND) function.

53. (Currently Amended) The optical logic circuit of claim ~~47~~ 52, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

54. (Previously Presented) The optical logic circuit of claim 53, wherein the optical processor comprises NOT (inverter) gates and NOT AND (NAND) gates.

55. (Currently Amended) An optical logic gate performing an inversion function for an optical processor, comprising:

a substrate configured of a first material;

a patterned optical layer overlaying the substrate, the optical layer comprising a second material, the patterned optical layer comprising a plurality of optical conduits formed of the second material, at least two of the optical conduits are configured to receive optical input signals, each of the optical input signals provide coherent light inputs, at least one of the optical conduits provides optical output signals, and at least one of the at least two optical input signals is a constant coherent light input signal; and

an interference region coupled to at least two of the optical conduits that are configured to receive optical input signals, a predetermined axis in the interference region along which maximum interference of optical signals in the interference region occurs, the interference region is coupled to at least one of the optical conduits configured to provide optical output signals, and the optical conduit receiving output signals is positioned such that the predetermined axis is aligned with the optical conduit receiving the output, the maximum destructive interference being caused exclusively by the interaction between first and second light inputs,

wherein the interference region is formed of the second material and bounded on ~~its periphery~~ all sides by material other than the second material except where the first and second optical inputs and optical output are located, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the optical inputs and the optical output ~~the periphery being a single, outer periphery such that only the interference region is within the periphery~~ and the interference region is configured to provide a Boolean logic output signal based on one optical input signal that may selectively be turned on and off and the output signal having one of two intensities, either a substantially on or a substantially off intensity.

56. (Previously Presented) The optical logic gate of claim 55, wherein the optical logic gate provides a Boolean NOT function as output.

57. (Previously Presented) The optical logic gate of claim 55, further comprising:
at least three optical conduits configured to receive optical inputs.

58. (Currently Amended) The optical logic gate of claim 57, wherein the optical logic gate provides a Boolean NOT AND (NAND) function as output.

59. (Previously Presented) The optical logic gate of claim 55, wherein the first material comprises silicon (Si).

60. (Previously Presented) The optical logic gate of claim 55, wherein the second material comprises doped silicon (Si).

61. (Previously Presented) The optical logic gate of claim 55, wherein the first material comprises Gallium Arsenide (GaAs).

62. (Previously Presented) The optical logic gate of claim 55, wherein the second material comprises doped Gallium Arsenide (GaAs).

63. (Previously Presented) The optical logic gate of claim 55, wherein the optical input signal is generated by a Laser diode.

64. (Previously Presented) The optical logic gate of claim 55, wherein the optical input signal is generated by a semiconductor diode.

65. (Currently Amended) A method of performing and inversion function in an optical logic circuit with at least two optical input signals and an optical output signal ~~providing a Boolean logic optical output signal based on at least two optical input signals~~, comprising:

providing a first constant coherent light input signal to a first optical input such that the input signal is in an always on condition;

providing a plurality of optical pathways formed of optical transmission material patterned on a substrate material;

providing a second coherent light input signal, the second coherent light input signal being a coherent light input that is selectively turned on and off;

providing a distance between the plurality of optical pathways entering an interference region, the interference region being formed of the optical transmission material and bounded on ~~its periphery~~ all sides by material other than the optical transmission material except where the first and second optical inputs and optical output are located, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the optical inputs and the optical output ~~the periphery being a single, outer periphery such that only the interference region is within the periphery~~ and the interference region enabling interference of the first constant coherent light input signal and the second coherent light input signal when the coherent light input signal is turned on, the interference being caused exclusively by the interaction between the first constant coherent light input signal and the second coherent light input signal; and

providing an optical output signal, the optical output signal is based on the first constant coherent light input signal and the second coherent light input signal and ~~is~~ representative of a Boolean logic function, and the output signal having one of two intensities, either a substantially on or a substantially off intensity.

66. (Previously Presented) The method of claim 65, wherein the Boolean logic function is a NOT (inverter) gate.

67. (Previously Presented) The method of claim 65, wherein the Boolean logic function is a NOT AND (NAND) gate.

68. (Previously Presented) The method of claim 65, wherein the Boolean logic function is configured of NOT (inverter) gates or NOT AND (NAND) gates.

69. (Currently Amended) An optical logic circuit for performing an inversion, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate partially comprising a second material, the optical layer is patterned to provide a plurality of optical pathways, at least two optical pathways are configured to provide optical input signals, the optical input signals are coherent light inputs, and at least one optical pathway is configured to provide an optical output signal; and

an interference region, the interference region being formed of the second material and bounded on ~~its periphery~~ all sides by material other than the second material except where the first and second optical inputs and optical output are located, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the optical inputs and the optical output, ~~the periphery being a single, outer periphery such that only the interference region is within the periphery~~ and the interference region configured to selectively cause interference of wavefronts of light from the optical input signals entering the interference region, the location of a chosen line, ~~of many lines,~~ along which maximum destructive interference of wavefronts of light from the optical input signals entering the interference region is predicted based on the distance between the at least two optical pathways entering the interference region and the length of the interference region, the third optical pathway is positioned such that the chosen line, is aligned with the third optical pathway, the destructive maximum interference is produced along the chosen line in the interference

region during a predetermined combination of light inputs, the destructive maximum interference being caused exclusively by interaction between optical signals entering the interference region through the first, second and third optical pathways,

wherein the interference region is configured to provide a Boolean logic output signal based on the at least two coherent light input signals.

70. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region receives a first optical input that may be selectively turned on and off and a constant coherent light input.

71. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when a light signal is provided to the interference region through the coherent light input, the light signal being selected as on.

72. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region includes a second coherent light input that may be selectively turned on and off.

73. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region is configured to cause substantially no light exiting the interference region output when light is provided to the interference region through both the first optical pathway and the second optical pathway, and when no light is provided to both of the first and second optical pathways.

74. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT (inverter) function.

75. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT AND (NAND) function.

76. (Previously Presented) The optical logic circuit of claim 69, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

77. (Previously Presented) The optical logic circuit of claim 76 , wherein the optical processor is configured of NOT (inverter) gates or NOT AND (NAND) gates.

78. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is an XOR (exclusive OR) function.